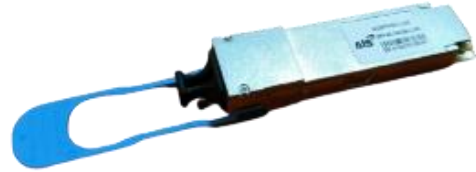


## 40G Base-LR4 QSFP+ Optical Transceiver Module

### Features:

- Compliant to the industry standard SFF-8436 QSFP+ Transceiver Specification
- Up to 11.2Gb/s data rate per wavelength
- 4 CWDM lanes MUX/DEMUX design
- Up to 20km transmission on single mode fiber (SMF)
- Operating case temperature: 0 to 70°C
- Maximum power consumption 3.5W
- LC duplex connector



### Description:

AIQSFP+ Transceiver is a high performance, cost effective module for serial optical data communication applications to 41.5Gb/s. The AIQSFP+ is designed to 40GBASE-LR4 of the IEEE P802.3ba standard for 20km links.

The module converts 4 input channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically demultiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface.

To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

### Compliance

- IEEE802.3ba 40GBASE-LR4
- SFF-8436 QSFP Specification
- InfiniBand Architecture QDR Specifications

### Absolute Maximum Ratings

Parameter	Symbols	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40	-	+85	°C	
Operating Temperature	Top	0		70		
Operating Relative Humidity	RH	0	-	85	%	
3.3V Supply Voltage	VCC	-0.5	-	+3.6	V	



## Recommended Operating Conditions

Parameter	Symbols	Min	Typical	Max	Unit	Notes
Case temperature	Tc	0	-	+70	°C	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate			41.25		Gbps	
Receiver Differential Data Output Load		90	100	110	Ohms	
Logic Input Voltage High	Vih	2		Vcc+0.3	V	
Logic Input Voltage Low	Vil	-0.3		0.8	V	
Two wire Serial Interface Clock Rate			100	400	KHz	
Power Noise and Ripple				50	mVpp	
Fiber Length				10	km	
Power Dissipation	PD			3.5	W	
Transceiver Power Supply Current				1008	mA	

## Optical, Electrical Characteristic

Parameter	Symbols	Min	Type	Max	Unit	Notes
Wavelength $\lambda_0$	$\lambda_0$	1264.5	1271	1277.5	nm	
Wavelength $\lambda_1$	$\lambda_1$	1284.5	1291	1297.5	nm	
Wavelength $\lambda_2$	$\lambda_2$	1304.5	1311	1317.5	nm	
Wavelength $\lambda_3$	$\lambda_3$	1324.5	1331	1337.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Spectral width	SW			1.0	nm	
Average power, each lane(EOL)	TXP	-7		3	dBm	
Extinction Ratio	ER	3.5			dB	
Optical Modulation Amplitude	OMA	-4		3.5	dBm	
Launch Power in OMA minus TDP, each lane		-4.8			dBm	
Difference in Power between any two lanes				6.5	dB	

Parameter	Symbols	Min	Type	Max	Unit	Notes
Wavelength $\lambda_0$	$\lambda_0$	1264.5	1271	1277.5	nm	
Wavelength $\lambda_1$	$\lambda_1$	1284.5	1291	1297.5	nm	
Wavelength $\lambda_2$	$\lambda_2$	1304.5	1311	1317.5	nm	
Wavelength $\lambda_3$	$\lambda_3$	1324.5	1331	1337.5	nm	
Max Input power		2.3			dBm	
Sensitivity,each lane				-11.5	dBm	

Stressed Receiver Sensitivity(OMA、EOL) ,each lane				-9.6	dBm	
Receiver Reflectance				-26	dBm	
Rx_Loss assert	LOSA	-30			dBm	
Rx_LossDe_assert	LOSD			-14	dBm	
LOS Hysteresis		0.5			dB	
Rx LOS in signal or RSSI			RSSI		-	

Digital Diagnostic Function						
Parameter	Symbols	Min	Type	Max	Unit	Notes
Temperature DDMaccuracy	DMI_Temp	-5		+5	°C	
Supply voltage DDMaccuracy	DMI_VCC	-5%		+5%	V	
Rx power DDMaccuracy	DMI_Rx	-3		+3	dB	
Bias current DDM accuracy	DMI_Ibias	-10%		+10%	mA	
Tx power DDM accuracy	DMI_Tx	-3		+3	dB	

### Pin-out Definitions

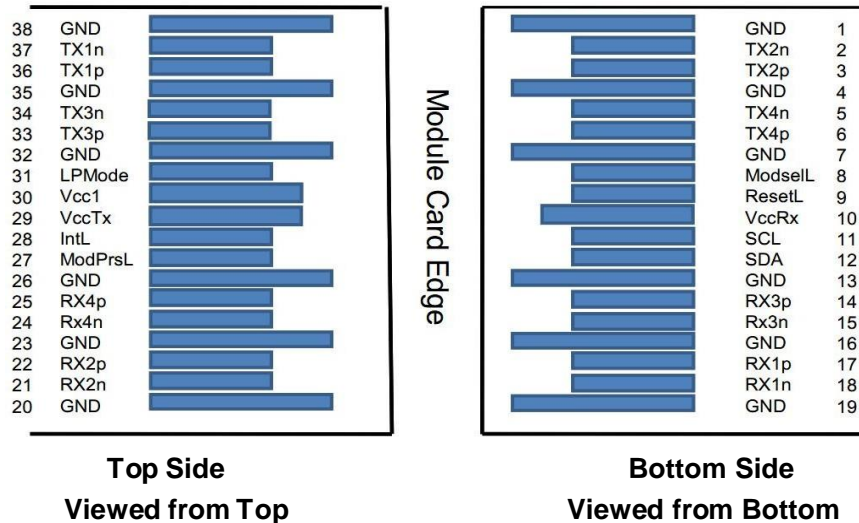


Figure 1 – QSFP+ MSA-compliant 38-pin connector

### Pin Description

Pin	Name	Description	Notes
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	



6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	



## Recommended Interface Circuit

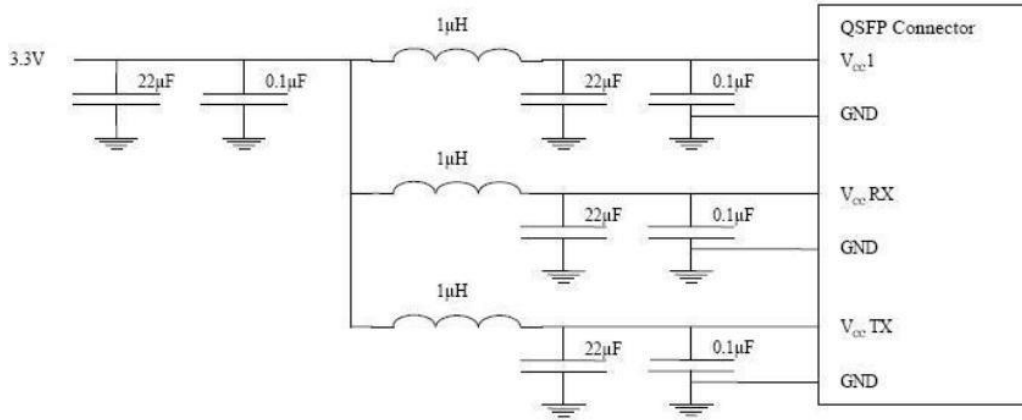


Figure2 - Host Board Power Supply Filtering

## EEPROM Serial ID Memory Contents

2-Wire Serial Address 1010000x	
Lower Page 00h	
0 Identifier	
1- 2 Status	
3- 21 Interrupt Flags	
22- 33 Free Side Device Monitors	
34- 81 Channel Monitors	
82- 85 Reserved	
86- 98 Control	
99 Reserved	
100-104 Hardware Interrupt Pin Masks	
105-106 Vendor Specific	
107 Reserved	
108-110 Free Side Device Properties	
111-112 Assigned for use by PCI Express	
113 Free Side Device Properties	
114-118 Reserved	
119-122 Password Change Entry Area (Optional)	
123-126 Password Entry Area (Optional)	
127 Page Select Byte	

Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		176-223 Channel Thresholds
	130-131 Application Code Entry 0		224 Tx EQ & Rx Emphasis Magnitude ID
	132-133 Application Code Entry 1		225 RX output amplitude indicators
192-223 Extended ID	134-253 other entries		226-241 Channel Controls
224-255 Vendor Specific ID	254-255 Application Code Entry TL	242-251 Channel Monitor Masks	
		252-255 Reserved	

Figure 3- QSFP+ Memory Map